# PXIe-5412

# Static Digital I/O Module

# User Manual


User Manual Version: V1.0.0

Revision Date: Dec. 22, 2025

# 1. PXIe-5412 Specifications

## 1.1 Overview

PXIe-5412 is a 96 channels static digital I/O module. 96 digital channels can use software to program data direction. The signal level supports 2 options: 3.3V and 5V, and can be switched individually for each port.Data sequence can be freely combined by software.

Please download JYTEK <JYPEDIA>, you can quickly inquire the product prices, the key features and available accessories..

## 1.2 Main Features

- 96-CH static DIO
- Independent data direction control of each channel
- Support 3.3V/5V level
- Support individual level switching for each port
- Debounce Filter
- Change Detection
- Watchdog Timer
- Programmable Power-Up States

## 1.3 Hardware Specifications

**Basic**

**DIO**

| | |
|---|---|
| Number of channels | 96 I/O |
| Compatibility | COMS input<br>Push-pull outputs |
| Power-on state | Input: Floating/Pull-up/Pull-down<br>Output: High/Low |
| Programable logic level | 3.3 V, 5 V |
| Data transfers | Interrupts， programmed I/O |
| I/O connector | SCSI-100 |
| Pull resistor | Pull-up resistor：100 kΩ， typical<br>Pull-down resistor：70 kΩ， typical |
| Input voltage protection | -3 V~+20 V |
| Input/Output Latency | ＜0.03ms |
| Programmable power-up states response time | 180ms |
| +5 V power available at I/O connector (pins 49 and 99) | +4 V to +5 V, 1 A, maximum |

Table 1 DIO Basic

**Digital Logic Levels**

**Input Signals**

| | |
|---|---|
| Input voltage （$V_{in}$） | 0V ~ VDD* |
| Input logic high voltage （$V_{IH}$） | 0.7VDD* ~ VDD |
| Input logic low voltage （$V_{IL}$） | 0V ~ 0.3VDD |

*: VDD is 3.3V or 5V software selectable by port.

**Output Signals**

| | |
|---|---|
| High-level Output current （$I_{OH}$） | 10mA |
| Low-level Output current （$I_{OL}$） | 25mA |
| Output voltage （$V_{out}$） | 0 V ~ VDD |
| Output high voltage （$V_{OH}$） | VDD-0.4 V~ VDD |
| Output low voltage （$V_{OL}$） | 0~0.3V |

**Do Output Mode**

| DO Output Mode | DO Value | Output Status |
|---|---|---|
| Push-Pull | 1 | High Level (VDD) |
| | 0 | Low Level (GND) |

Table 2 Do Output Mode

## Physical and Environment

**Bus Interface**

| | | |
|---|---|---|
| Bus interface | PXIe standard | x4 PXI Express peripheral module Specification V1.0 compliant |
| | Slot supported | x1 and x4 PXI Express or PXI Express hybrid slots |

**Physical Characteristics**

| | |
|---|---|
| Dimensions | 3U PXIe |
| Weight | 213.6 g |

**Operating Temperature**

| | |
|---|---|
| Ambient temperature range | 0℃~50℃ |
| Relative humidity range | 20% to 80%, none-condensing |

**Storage Environment**

| | |
|---|---|
| Ambient temperature range | -20 °C to 50 °C |
| Relative humidity range | 10% to 90%, none-condensing |

Table 3 Physical and Environment

Order Information

PXIe-5412 (PN: JY1461945-01)

96-Channel, 3.3V/5 V, CMOS PXIe Statistic Digital I/O Module

Accessories

- ACL-1020100-1 1M 100pin SCSI twisted pair cable (PN: JY4910923-01)
- ACL-1020100-2 2M 100pin SCSI twisted pair cable (PN: JY7155665-01)

Terminal Block

- DIN-100-1 100-Pin SCSI Terminal block (PN: JY7739162-01)

# Table of Contents

# 2. Introduction

This chapter presents the information how to use this manual and operate the module if you are already familiar with Microsoft Visual Studio and C# programming language.

## 2.1 Overview

The PXIe-5412 is a 96 channels static digital I/O module. PXIe-5412 provides 96 channels of configurable digital input and output, and the main parameters are shown in Table 1 below.

| | |
|---|---|
| Number of DIO channels | 96 configurable I / O per channel |
| Voltage Level | 3.3 V / 5 V |
| Input/Output Latency | ＜0.3ms |

Table 1 PXIe-5412 products Main Features

PXIe-5412 is a 96 channels static digital I/O module. The direction of all the 96 digital channels can be programmed by software. The signal level supports 2 options: 3.3V and 5V, and can be switched individually for each port. Data sequence can be modified by software. The module is designed for static digital signal input/output applications, supporting software-based digital input status polling and digital output status setting.

## 2.2 Abbreviation

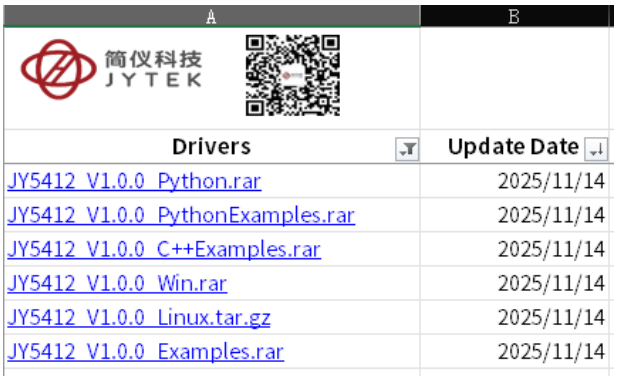
DI: Digital Input

DO: Digital Output

DAQ: Data AcQuisition

## 2.3 Learn by Example

JYTEK has added **Learn by Example** in this manual. We provide many sample programs for this device. Please download and install the sample programs for this device. You can download a JYPEDIA excel file from our web www.jytek.com. Open JYPEDIA and search for JY5412 in the driver sheet, select **JY5412_Examples.zip**. This will lead you to download the sample program for this device. In addition to the download information, JYPEDIA also has a lot of other valuable information, JYTEK highly recommend you use this file to obtain information from JYTEK.



| Drivers | Update Date |
|---|---|
| JY5412_V1.0.0_Python.rar | 2025/11/14 |
| JY5412_V1.0.0_PythonExamples.rar | 2025/11/14 |
| JY5412_V1.0.0_C++Examples.rar | 2025/11/14 |
| JY5412_V1.0.0_Win.rar | 2025/11/14 |
| JY5412_V1.0.0_Linux.tar.gz | 2025/11/14 |
| JY5412_V1.0.0_Examples.rar | 2025/11/14 |

Figure 1 JYPEDIA Information

In a **Learn by Example** section, the sample program is in bold style such as **Digital Input--> Winform DI SinglePoint**; the property name in the sample program is also in bold style such as **Channels**; the technical names used in the manual is in italic style such as *DITerminal*. You can easily relate the property names in the example program with the manual documentation.

In a Learn by Example section, the experiment is set up as follow. One PXIe-5412 card is plugged in a desktop computer. The PXIe-5412 is connected to a DIN-100-1 terminal block. A signal source is also connected to the same terminal block.

# 3. Hardware Specifications

## 3.1 System Diagram

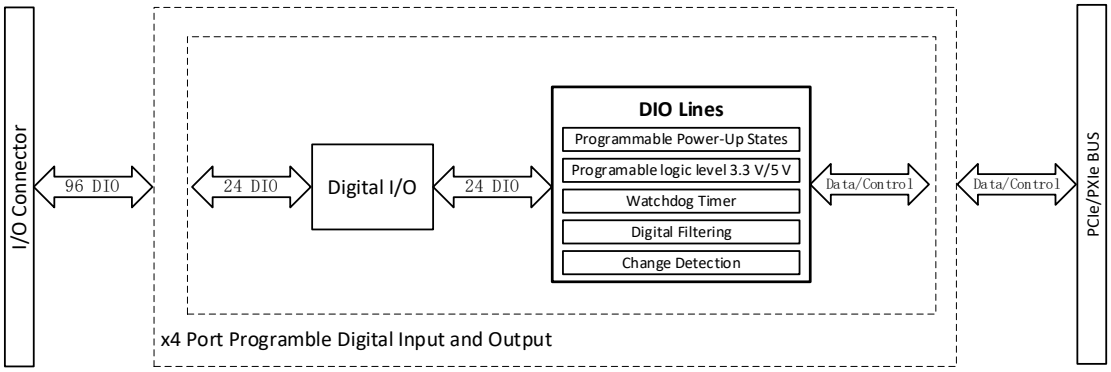



Figure 2 PXIe-5412 System Block Diagram

Figure 2 shows the system architecture of PXIe-5412. This module provides 4 ports of programmable digital input/output , supporting separate switching of logic levels between 3.3V and 5V by port. The module has programmable power on status, watchdog timer, digital filtering, and change detection functions to ensure signal stability and reliable monitoring, suitable for high demand industrial control and testing applications..

## 3.2 Specification

### 3.2.1 Digital IO

| | |
|---|---|
| Number of channels | 96 I/O |
| Compatibility | COMS input<br>Push-pull outputs |
| Power-on state | Input : Floating/Pull-up/Pull-dowr<br>Output : High/Low |
| Programable logic level | 3.3 V, 5 V |
| Data transfers | Interrupts，programmed I/O |
| I/O connector | SCSI-100 |
| Pull resistor | Pull-up resistor：100 kΩ，typical<br>Pull-down resistor：70 kΩ，typical |
| Input voltage protection | -3 V~+20 V |
| Input/Output Latency | < 0.3ms |
| Programmable power-up states response time | 180ms |
| +5 V power available at I/O connector (pins 49 and 99) | +4 V to +5 V, 1 A, maximum |
| | |

Table 2 Digital IO

### 3.2.2 Digital Logic Levels

| | | |
|---|---|---|
| Input Signals | Input voltage （$V_{in}$） | 0V ~ VDD |
| | Input logic high voltage （$V_{IH}$） | 0.7 * VDD ~ VDD |
| | Input logic low voltage （$V_{IL}$） | 0V ~ 0.3 * VDD |
| Output Signals | High-level Output current （$I_{OL}$） | 10mA |
| | Low-level Output current （$I_{OL}$） | 25mA |
| | Output voltage （$V_{out}$） | 0 V ~ VDD |
| | Output high voltage （$V_{OL}$） | VDD-0.4 V~ VDD |
| | Output low voltage （$V_{OL}$） | 0~0.3V |

Table 3 Digital Logic Levels

Physical Characteristics

**Physical Characteristics**

| | |
|---|---|
| Dimensions | 3U PXIe |
| Weight | 213.6 g |

**Bus Interface**

| | | |
|---|---|---|
| Bus interface | PXIe standard | x4 PXI Express peripheral module Specification V1.0 compliant |
| | Slot supported | x1 and x4 PXI Express or PXI Express hybrid slots |

Table 4 Physical Characteristics

**Operating Environment**

| | |
|---|---|
| Ambient temperature range | 0°C~50°C |
| Relative humidity range | 20% to 80%, none-condensing |

**Storage Environment**

| | |
|---|---|
| Ambient temperature range | -20 °C to 50 °C |
| Relative humidity range | 10% to 90%, none-condensing |

Table 5 Input Protection

### 3.2.3 Do Output Mode

| DO Output Mode | DO Value | Output Status |
|---|---|---|
| Push-Pull | 1 | High Level (VDD) |
| | 0 | Low Level (GND) |

Table 6 DO Output Mode

## 3.3 Pin Definition

| Pin Number | Signal | Pin Number | Signal |
|---|---|---|---|
| 1 | P3.23 | 51 | P2.23 |
| 2 | P3.22 | 52 | P2.22 |
| 3 | P3.21 | 53 | P2.21 |
| 4 | P3.20 | 54 | P2.20 |
| 5 | P3.19 | 55 | P2.19 |
| 6 | P3.18 | 56 | P2.18 |
| 7 | P3.17 | 57 | P2.17 |
| 8 | P3.16 | 58 | P2.16 |
| 9 | P3.15 | 59 | P2.15 |
| 10 | P3.14 | 60 | P2.14 |
| 11 | P3.13 | 61 | P2.13 |
| 12 | P3.12 | 62 | P2.12 |
| 13 | P3.11 | 63 | P2.11 |
| 14 | P3.10 | 64 | P2.10 |
| 15 | P3.9 | 65 | P2.9 |
| 16 | P3.8 | 66 | P2.8 |
| 17 | P3.7 | 67 | P2.7 |
| 18 | P3.6 | 68 | P2.6 |
| 19 | P3.5 | 69 | P2.5 |
| 20 | P3.4 | 70 | P2.4 |
| 21 | P3.3 | 71 | P2.3 |
| 22 | P3.2 | 72 | P2.2 |
| 23 | P3.1 | 73 | P2.1 |
| 24 | P3.0 | 74 | P2.0 |
| 25 | P1.23 | 75 | P0.23 |
| 26 | P1.22 | 76 | P0.22 |
| 27 | P1.21 | 77 | P0.21 |
| 28 | P1.20 | 78 | P0.20 |
| 29 | P1.19 | 79 | P0.19 |
| 30 | P1.18 | 80 | P0.18 |
| 31 | P1.17 | 81 | P0.17 |
| 32 | P1.16 | 82 | P0.16 |
| 33 | P1.15 | 83 | P0.15 |
| 34 | P1.14 | 84 | P0.14 |
| 35 | P1.13 | 85 | P0.13 |
| 36 | P1.12 | 86 | P0.12 |
| 37 | P1.11 | 87 | P0.11 |
| 38 | P1.10 | 88 | P0.10 |
| 39 | P1.9 | 89 | P0.9 |
| 40 | P1.8 | 90 | P0.8 |
| 41 | P1.7 | 91 | P0.7 |
| 42 | P1.6 | 92 | P0.6 |
| 43 | P1.5 | 93 | P0.5 |
| 44 | P1.4 | 94 | P0.4 |
| 45 | P1.3 | 95 | P0.3 |
| 46 | P1.2 | 96 | P0.2 |
| 47 | P1.1 | 97 | P0.1 |
| 48 | P1.0 | 98 | P0.0 |
| 49 | +5V | 99 | +5V |
| 50 | GND | 100 | GND |

Table 7 Pin Definition

## 3.4 Front Pannel Connection

Figure 3 Front Pannel Connection

## 3.5 Cable

| | |
|---|---|
| Cable | ACL-1020100-1<br>ACL-1020100-2 |
| TB | DIN-100-1 |

Table 8 Cable

# 4. Software

## 4.1 System Requirements

PXIe-5412 can be used in a Windows or a Linux operating system.

Microsoft Windows: Windows 7 32/64 bit, Windows 10 32/64 bit.

Linux Kernel Versions: There are many Linux versions. It is not possible JYTEK can support and test our devices under all different Linux versions. JYTEK will at the best support the following Linux versions.

| Linux Version |
| --- |
| **Ubuntu LTS** |
| 16.04： 4.4.0-21-generic(desktop/server) |
| 16.04.6：4.15.0-45-generic(desktop) 4.4.0-142-generic(server) |
| 18.04： 4.15.0-20-generic(desktop) 4.15.0-91-generic(server) |
| 18.04.4：5.3.0-28-generic (desktop) 4.15.0-91-generic(server) |
| **Localized Chinese Version** |
| 中标麒麟桌面操作系统软件（兆芯版）V7.0（Build61）: 3.10.0-862.9.1.nd7.zx.18.x86_64 |
| 中标麒麟高级服务器操作系统软件V7.0U6: 3.10.0-957.el7.x86_64 |

Table 9 Supported Linux Versions

## 4.2 System Software

When using the PXIe-5412 in the Windows environment, you need to install the following software from Microsoft website:

Microsoft Visual Studio Version 2015 or above,

.NET Framework version is 4.0 or above.

.NET Framework is coming with Windows 10. For Windows 7, please check .NET Framework version and upgrade to 4.0 or later version.

Given the limited resources, JYTEK only tested PXIe-5412 with .NET Framework 4.0 and Microsoft Visual Studio 2015. JYTEK relies on Microsoft to maintain the compatibility for the newer versions.

## 4.3 C# Programming Language

The default programming language of all the examples provided by JYTEK is Microsoft C#. This is Microsoft's recommended programming language in Microsoft Visual Studio and is particularly suitable for the test and measurement applications. C# is also a cross-platform programming language.

## 4.4 PXIe-5412 Series Hardware Driver

After installing the required application development environment as described above, you need to install the PXIe-5412 hardware driver.

JYTEK hardware driver has two parts: the shared common driver kernel software (FirmDrive) and the specific hardware driver.

Common Driver Kernel Software (FirmDrive): FirmDrive is the kernel software for all hardware products of JYTEK. You need to install the FirmDrive software before using any other JYTEK hardware products. FirmDrive only needs to be installed once. After that, you can install the specific hardware driver.

Specific Hardware Driver: Each JYTEK hardware has a specific C# hardware driver. This driver provides rich and easy-to-use C# interfaces for users to operate various PXIe-5412 functions. JYTEK has standardized the ways which JYTEK and other vendor's DAQ boards are used by providing a consistent user interface, methods, properties and enumerations in the object-oriented programming environment. Once you get yourself familiar with how one JYTEK DAQ card works, you should be able to know how to use all other DAQ hardware by using the same methods.

## 4.5 Install the SeeSharpTools from JYTEK

To efficiently and effectively use PXIe-5412, you need to install a set of free C# utilities, SeeSharpTools from JYTEK. The SeeSharpTools offer rich user interface functions that you will find convenient in developing your applications. They are also needed to run the examples that come with PXIe-5412 hardware. Please register and down load the latest SeeSharpTools from our website, www.jytek.com.

## 4.6 Running C# Programs in Linux

Most C# written programs in Windows can be run by MonoDevelop development system in a Linux environment. You would develop your C# application in Windows using Microsoft Visual Studio. Once it is done, run this application in the MonoDevelop environment. This is JYTEK's recommended way to run your C# programs in a Linux environment.

If you want to use your own Linux development system other than MonoDevelop, you can do it by using our Linux driver. However, JYTEK does not have the capability to support the Linux applications. JYTEK completely relies upon Microsoft to maintain the cross-platform compatibility between Windows and Linux using MonoDevelop.

# 5. Operating PXIe-5412

This chapter mainly introduces the related operation guide of PXIe-5412, mainly including the definition and usage of driver.

JYTEK provides a large number of exsamples, online help and documents to help you use the PXIe-5412. We strongly recommend that you read these examples before writing your own application. In many cases, the examples can also help a lot of actual test projects start quickly.

## 5.1 Quick Start

After you have installed the driver software and the SeeSharpTools, you are ready to use Microsoft Visual Studio C# to operate the PXIe-5412.

If you are already familiar with Microsoft Visual Studio C#, the quickest way to use PXIe-5412 is to go through our extensive examples. We provide source code of our examples. In many cases, you can modify the source code and start to write your applications.

## 5.2 Programmable Multifunctional I / O

PXIe-5412 supports powerful programmable I / O functions and 96 channels of DI / DO. For more information, refer to examples.

### 5.2.1 Static DI/ DO

Programmable I/O function supports static digital input and output with 96 channels. User can access the I / O information through software polling.

### 5.2.2 Static DI Pull-Up/Pull-Down Resistors

PXIe-5412 has user-configurable pull-up and pull-down resistors. The DIO lines on the PXIe-5412 contains a software-selectable pull-down resistor (70 kΩ, typical)/pull-up resistor (100 kΩ, typical), or floating.

If you set the software to pull-down, the pull-down resistor pulls the DIO line low. If you set the software to pull-up, the pull-up resistor pulls the DIO line high. The pull setting that you set affects only the state of DIO lines that are configured for input. Each line can be independently configured.

## 5.3 Debounce Filter

Mechanical switches do not make clean make-or-break connections and the contacts can 'bounce' for a significant period of time before settling into a steady-state condition. This can confuse fast processors and make the physical interface difficult to design and the software interface difficult to make reliable.

The PXIe-5412 employs dedicated circuitry to implement hardware debouncing for switch closures. All 96 lines can be connected to this hardware debouncing circuitry.By default, the debounce filter function of the PXIe-5412 is disabled. As needed, enable debounce filter on as many input lines as possible.

You can configure the input lines to pass through the debounce filter and control the time interval used by the filter. The filter blocks pulses shorter than the specified time interval and allows pulses longer than the specified time interval to pass through.

Internally, the debounce filter uses a filter clock and a debounce counter.

- filter clock frequency :3 selectable ranges (10 MHz/100 kHz/1 kHz)
- debouce counter range : 0~255

Each port shares a common filter clock frequency, while each line can be independently configured for enablement status and debounce counter value—this configuration covers a debounce pulse width range of 100 ns to 200 ms.

## 5.4 Change Detection

You can enable the PXIe-5412 DIO change detection circuitry to detect rising edges (0 to 1), falling edges (1 to 0), or both edges on selected input lines or on all input lines.

When an input change occurs, the PXIe-5412 generates an interrupt and notifies the software. The device reports which line has undergone the change and the state of that line at the time of the change. The rate of change detection depends on the software response time, which may vary across different systems.

Excessive change detections may affect system performance. Use digital filtering to minimize the effects of noisy input lines.

## 5.5 Watchdog Timer

The watchdog timer is a software-configurable feature designed to set critical outputs to a safe state in the event of software faults, system crashes, or any communication interruptions between the application and the PXIe-5412.

When the watchdog timer is enabled, and the PXIe-5412 does not receive a watchdog reset software command within the time specified for the watchdog timer, the outputs go to a user-defined safe state and remain in that state until one of the following occurs:

• The watchdog timer is disarmed by the application and new values are written.

• The computer is restarted.

The expiration signal that indicates an expired watchdog will continue to assert until the watchdog is disarmed. After the watchdog timer expires, the device doesn’t allow any digital writes until the watchdog timer is disarmed.

You can set the watchdog timer timeout period to specify the amount of time that must elapse before the watchdog timer expires. The counter on the watchdog timer is configurable up to $(2^{32} - 1) \times 20$ ns (approximately 86 seconds) before it expires. A watchdog timer can be set for all DIO lines.

## 5.6 Programmable Power-Up States

With the programmable power-on state, the device consistently powers on in a predictable state. The device's DIO lines offer flexible predefined power-on configurations to suit diverse application needs, including floating, pull-up, or pull-down input; push-pull output (configurable for high or low level); and selectable 3.3V or 5V logic levels.

# 6. Using PXIe-5412 in Other Software

While JYTEK's default application platform is Visual Studio, the programming language is C#, we recognize there are other platforms that are either becoming very popular or have been widely used in the data acquisition applications. Among them are Python, C++. This chapter explains how you can use PXIe-5412 card using one of this software.

## 6.1 Python

JYTEK provides and supports a native Python driver for PXIe-5412 cards. There are many different versions of Python. JYTEK has only tested in CPython version 3.5. There is no guarantee that JYTEK python drivers will work correctly with other versions of Python.

If you want to be our partner to support different Python platforms, please contact us.

## 6.2 C++

JYTEK internaly uses our C++ drivers to design the C# drivers. We recommend our customers to use C# drivers because C# platform deliver much better efficiency and performance in most situations. We also make our C++ drivers available. However, due to the limit of our resources, we do not actively support C++ drivers. You can download our C++ drivers from JYTEK's website. We welcome you report the bugs in our C++ drivers, but will not be able to guarantee that we can fix it within your expectation.

If you want to be our partner to support C++ drivers, please contact us.

# 7. About JYTEK

## 7.1 JYTEK China

Founded in June, 2016, JYTEK China is a leading Chinese test & measurement company, providing complete software and hardware products for the test and measurement industry. The company has evolved from re-branding and reselling PXI(e) and DAQ products to a fully-fledged product company. The company offers complete lines of PXI, DAQ, USB products. More importantly, JYTEK has been promoting open-sourced based ecosystem and offers complete software products. Presently, JYTEK is focused on the Chinese market. Our Shanghai headquarters and production service center have regular stocks to ensure timely supply; we also have R&D centers in Xi'an and Chongqing. We also have highly trained direct technical sales representatives in Shanghai, Beijing, Tianjin, Xi'an, Chengdu, Nanjing, Wuhan, Guangdong, Haerbin, and Changchun. We also have many patners who provide system level support in various cities.

## 7.2 JYTEK Software Platform

JYTEK has developed a complete software platform, SeeSharp Platform, for the test and measurement applications. We leverage the open sources communities to provide the software tools. Our platform software is also open sourced and is free, thus lowering the cost of tests for our customers. We are the only domestic vendor to offer complete commercial software and hardware tools.

## 7.3 JYTEK Warranty and SupportServices

With our complete software and hardware products, JYTEK is able to provide technical and sales services to wide range of applications and customers. In most cases, our products are backed by a 1-year warranty. For technical consultation, pre-sale and after-sales support, please contact JYTEK of your country.

# 8. Statement

The hardware and software products described in this manual are provided by JYTEK China, or JYTEK in short.

This manual provides the product review, quick start, some driver interface explanation for PCIe/PXIe-5412 static digital I/O module. The manual is copyrighted by JYTEK.

No warranty is given as to any implied warranties, express or implied, including any purpose or non-infringement of intellectual property rights, unless such disclaimer is legally invalid. JYTEK is not responsible for any incidental or consequential damages related to performance or use of this manual. The information contained in this manual is subject to change without notice.

While we try to keep this manual up to date, there are factors beyond our control that may affect the accuracy of the manual. Please check the latest manual and product information from our website.

Shanghai Jianyi Technology Co., Ltd.

Address: Room 201, Building 3, NO.300 Fangchun Road, Shanghai.

Post Code：201203

Tel：021-5047 5899

Website：www.jytek.com